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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/661,016	Applicant(s) GROEN ET AL.
	Examiner Vineeta S. Panwalkar	Art Unit 2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-26 and 28-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-26* is/are allowed.

6)☒ Claim(s) *1-5,8,9,12,14-16,28-33,36,37,40-42,44 and 47* is/are rejected.

7)☒ Claim(s) *6,7,10,11,17,18,34,35,38,39,43,46 and 48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1a. Applicant's arguments filed 7/2/07 regarding the fact that the transceiver disclosed by Schneider (US 6201829) is not a programmable transceiver have been fully considered but they are not persuasive. (See Figs. 4 and 5, transceiver 30. See column 4, lines 54-60 and column 7, lines 27-35. The transceiver is capable of operating in different modes based on an external MODE signal and is hence it is interpreted as being programmable.

1b. Applicant's arguments about Schneider's transceiver not being multi-gigabit transceiver, see remarks, filed 7/2/07, with respect to the rejection(s) of claim(s) 1-5, 8, 9, 12, 14-16, 20, 21,23, 24, 26-33, 36, 37, 40-42, 44, 45 and 47 are rejected as obvious under 35 U.S.C. §103.under have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tans.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1, 2, 4, 5, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider in view of Homann (US 2001/0009553 A1, previously cited), hereinafter, Homann.

2a. Regarding claim 1, Schneider discloses a programmable gigabit transceiver (Figs. 4 and 5, transceiver 30. See column 4, lines 54-60 and column 7, lines 27-35. The transceiver is adapted to interface between high-speed serial data having a 1.065GigaHertz data rate (hence interpreted as gigabit transceiver) and

can operate in different modes based on an external MODE signal (hence it is interpreted as being programmable)) comprising:

- a module operably coupled to convert transmit parallel data into transmit serial data in accordance with a programmed serialization setting (Fig. 5, serializer 52 performs claimed parallel to serial conversion (See column 7, lines 49-52)) and to convert receive serial data into receive parallel data in accordance with a programmed deserialization setting ((Fig. 5, deserializer 58 performs claimed parallel to serial conversion (See column 8, lines 1-5)));
- module operably coupled to convert transmit data words into the transmit parallel data in accordance with a transmit interface setting and to convert the receive parallel data into receive data words in accordance with a receive interface setting (Column 1, line 65 – column 2, line 15. 8bit information (claimed transmit data word) is encoded into a 10bit transmission character (claimed transmit parallel data) over the system's parallel architecture. Similarly, at the receiver, the 10 bit transmission character (obtained after deserialization, interpreted as claimed receive parallel data) is decoded into an 8-byte recognizable by computer architectures (claimed receive data words). Fig. 4. The Fibre Channel protocol device 32 performs the encoding and is interpreted as claimed module. See column 6, lines 40-65);
- programmable interface operably to convey the receive data words and to convey the transmit data words in accordance with a programmed logic interface setting (See column 1, line 25- column 2, line 26. In accordance with

the Fibre-Channel physical and signaling interface specification, defined in ANSI X3.230-1994, information to be transmitted over a fibre wire or cable is encoded, 8 bits at a time, into a 10-bit Transmission Character which is subsequently serially transmitted by bit. Data provided over a typical computer system's parallel architecture is encoded and framed such that each data byte (8-bits from the point of view of the computer system) is formed into a Transmission Character in accordance with the Fibre-Channel 8B/10B transmission code. See Fig. 4. Since the Fibre Channel protocol device 32 performs the encoding, it inherently interfaces the data to be transmitted (claimed transmit data words) to the transceiver by performing the 8B/10B encoding on the data to be transmitted (to form claimed transmit parallel data). Similarly, the encoded received data (claimed received parallel words) is decoded by the Fibre Channel protocol device 32 and delivered in decoded form (claimed received data words). Thus, the Fibre-Channel protocol device is interpreted as claimed programmable interface. See column 6, lines 40-65); and

- control module operably coupled to generate the programmed serialization setting, the programmed deserialization setting, the receive interface setting, the transmit interface setting, and the logic interface setting based on a desired mode of operation for the programmable gigabit transceiver (See Figs. 4 and 5; column 7, lines 27-35. MODE is an external signal, typically asserted via controller circuitry (claimed control module) operating under

software or firmware program control, in response to certain predetermined conditions).

Thus, Schneider discloses all the limitations of the high-speed transceiver claimed, but fails to explicitly mention the terms programmable physical media attachment (PMA) or programmable physical coding sublayer (PCS) and whether the transceiver may be a multi-gigabit transceiver.

In the same field of endeavor, however, Homann discloses a high speed transceiver comprising physical coding sublayer (PCS) device for conversion of data to be transmitted or received to lower layer signals and a physical media attachment device for converting lower layer signals to media signals.(See Paragraphs [0025] and [0026]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the terms programmable physical media attachment (PMA) and programmable physical coding sublayer (PCS) (as disclosed by Homann) to describe modules that perform the claimed functions (as shown by Schneider) so as to conform to naming standards. Further, it would have been obvious to a person of ordinary skill in the art to use a well known multi-gigabit transceiver[1] instead of the gigabit transceiver shown by Schneider in order to increase system capacity.

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[1] References showing multi-gigabit transceivers: Trans (US 2001/0038674 A1); Buchwald et al. (US 2002/0034222 A1)

2b. Regarding claim 2, Schneider and Homann show all the limitations claimed (See 2a above).

Schneider further shows the programmable gigabit transceiver wherein the programmable module comprises:

- a programmable receiver module operably coupled to deserialize the receive serial data in accordance with the programmed deserialization setting to produce the receive parallel data; and (Fig. 5, deserializer 58 performs claimed deserialization in the receiver section 44 (claimed receiver module) of transceiver. See column 8, lines 1-5);
- a programmable transmitter module operably coupled to serialize the transmit parallel data in accordance with a programmed serialization setting to produce the transmit serial data. (Fig. 5, serializer 52 performs claimed serialization in the transmitter section 38 (claimed transmitter module) of transceiver. See column 7, lines 49-52).

2c. Regarding claim 4, Schneider and Homann show all the limitations claimed (See 2b above).

Schneider further shows the programmable gigabit transceiver wherein the programmable PMA transmitter module further comprises:

- phase locked loop operably coupled to produce timing signals in accordance with the programmed serialization setting (See Fig. 4 and column 6, line 46 –

column 7, line 8. Transmitter phase locked loop 40 produces the required 1.0625 GHz serial signal clock (claimed timing signal) defining the data rate of the high speed output, i.e. in accordance with the programmed serialization setting, as claimed);

- parallel-to-serial module operably coupled to convert the transmit parallel data into the transmit serial data based on the timing signals, wherein data width of the transmit parallel data and rate of the transmit serial data are set in accordance with the programmed serialization setting; (See Fig. 4 and column 7, lines 48-58. Once a 10-bit transmission character is latched into the transmitter section 38 through input latch 50, the transmission character is serialized in serializer 52, operating in accordance with a 1.0625 GHz signal provided by the transmitter PLL 40. Thus, parallel data and rate of the transmit serial data are set in accordance with the 1.0625 GHz timing signal. Since the 1.0625 GHz timing signal is set in accordance with the programmed serialized setting, data width of the transmit parallel data and rate of the transmit serial data are also set in accordance with the programmed serialization setting, as claimed); and
- driver operably coupled to drive the transmit serial data on to a transmission line, wherein drive level of the driver and pre-emphasis settings of the driver is set in accordance with the programmed serialization setting (See Fig. 4 and column 7, lines 48-58. Once serialized, a 1.0625 GHz serial datastream is directed out of the transmitter section 38 through an output buffer 54

(interpreted as claimed driver) which matches the serial data signal characteristics to the requirements of the Fibre Channel transmission bus (claimed transmission line), i.e. Output buffer 54 performs the function of claimed driver by outputting data onto the Fibre Channel transmission bus (claimed transmission line) in accordance with the serial data signal characteristics (claimed serialized setting)).

2d. Regarding claim 5, Schneider and Homann show all the limitations claimed (See 2a above).

Schneider further shows the programmable gigabit transceiver wherein the programmable module comprises:

- a programmable receive module operably coupled to convert the receive parallel data into receive data words in accordance with the receive interface setting; and a programmable PCS transmit module operably coupled to convert the transmit data words into the transmit parallel data in accordance with the transmit interface setting. (Column 1, line 65 – column 2, line 15. At the transmitter (claimed transmit module), 8bit information (claimed transmit data word) is encoded into a 10bit transmission character (claimed transmit parallel data) over the system's parallel architecture. Similarly, at the receiver (claimed receive module), the 10 bit transmission character (obtained after deserialization, interpreted as claimed receive parallel data) is decoded into an 8-byte recognizable by computer architectures (claimed receive data

words). Fig. 4. The Fibre Channel protocol device 32 performs the encoding. See column 6, lines 40-65).

2e. Regarding claim 8, Schneider and Homann show all the limitations claimed (See 2a above).

Since Schneider discloses a programmable gigabit transceiver (See 2a above), memory to store the programmed settings is inherent.

Thus, Schneider discloses all the limitations of the high-speed transceiver claimed, but fails to explicitly mention the terms programmable physical media attachment (PMA) or programmable physical coding sublayer (PCS).

In the same field of endeavor, however, Homann discloses a high speed transceiver comprising physical coding sublayer (PCS) device for conversion of data to be transmitted or received to lower layer signals and a physical media attachment device for converting lower layer signals to media signals.(See Paragraphs [0025] and [0026]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the terms programmable physical media attachment (PMA) and programmable physical coding sublayer (PCS) (as disclosed by Homann) to describe modules that perform the claimed functions (as shown by Schneider) so as to conform to naming standards. It would have also been obvious to a person of ordinary skill in the art to use separate memory registers for the PMA and PCS settings,

because this would ensure dedicated registers for each module, resulting in faster and easier memory access.

2f. Regarding claim 9, Schneider and Homann show all the limitations claimed (See 2e above).

Schneider further shows the control module further functions to:

- receive a programming setting that indicates the desired mode of operation for the programmable gigabit transceiver (See Figs. 4 and 5; column 7, lines 27-35. MODE is an external signal, typically asserted via controller circuitry (claimed control module) operating under software or firmware program control, in response to certain predetermined conditions. Thus, MODE indicates the desired mode of operation of the programmable gigabit transceiver).
  - convert the programming setting into the programmed serialization setting, the programmed deserialization setting, the receive interface setting, the transmit interface setting, and the logic interface setting (Since the gigabit transceiver operates based on the received MODE signal, the MODE signal inherently gets converted into serialization setting, deserialization setting and the interface setting, so as to control the serializer , deserializer and interface);

Since Schneider discloses a programmable gigabit transceiver (See 2a above), memory to store the programmed settings is inherent.

Thus, Schneider discloses all the limitations of the high-speed transceiver claimed, but fails to explicitly mention the terms programmable physical media attachment (PMA) register or programmable physical coding sublayer (PCS) register.

In the same field of endeavor, however, Homann discloses a high speed transceiver comprising physical coding sublayer (PCS) device for conversion of data to be transmitted or received to lower layer signals and a physical media attachment device for converting lower layer signals to media signals.(See Paragraphs [0025] and [0026]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the terms programmable physical media attachment (PMA) and programmable physical coding sublayer (PCS) (as disclosed by Homann) to describe modules that perform the claimed functions (as shown by Schneider) so as to conform to naming standards. It would have also been obvious to a person of ordinary skill in the art to use separate memory registers for the PMA and PCS settings, because this would ensure dedicated registers for each module, resulting in faster and easier memory access.

3. Claims 3, rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider in view of Homann as applied to claims 2 and 23 above, and further in view of Phanse (US 6798828 B1, previously cited), hereinafter, Phanse.

3a. Regarding claim 3, Schneider and Homann disclose all the limitations claimed (See 2b above).

Schneider further discloses the programmable gigabit transceiver wherein the programmable receiver module further comprises:

data and clock recovery module operably coupled to recover data and a clock receive serial data to produce recovered data and a recovered clock, respectively, wherein the data and clock recovery module includes a programmable phase locked loop that is programmed in accordance with the programmed deserialization setting; and serial-to-parallel module operably coupled to convert the recovered data into the receive parallel data, wherein rate of the receive parallel data and width of the receive parallel data are set in accordance with the programmed deserialization setting. (A receiver section 44 is coupled to a high speed serial data input 46 and further comprises a receiver phase lock loop 48 (claimed data and clock recover module) which locks on to a 1.0625 GHz incoming serial signal and recovers a high speed serial clock and data. Serial data is converted into 10-bit parallel data (interpreted as claimed serial-to-parallel module) and the recovered parallel data is provided to the protocol device 32 over the 10-bit wide parallel TTL data receiver bus 36. See Fig 5 and column 7, lines 8-15).

Thus, Schneider and Homann disclose all the limitations claimed, but fail to explicitly disclose the claimed analog from end.

However, in the same field of endeavor, Phanse shows a gigabit rate transceiver with an analog front end operably coupled to:

- amplify and equalize the receive serial data to produce amplified and equalized receive serial data(Phanse's analog front end comprises an automatic gain control (AGC) circuit capable of receiving the reduced-echo incoming analog signal and amplifying the reduced-echo incoming analog signal by an adjustable gain factor (thus interpreted as programmable amplification, as claimed) to thereby produce an amplified incoming analog signal and an adaptive analog equalization filter capable of receiving the incoming amplified analog signal and amplifying a first high frequency component of the amplified incoming analog signal to thereby produce an analog filtered incoming signal Column 3, lines 45-68).

Thus, it would have been obvious to a person of ordinary skill in the art to use the analog front-end disclosed by Phanse because it improves performance of gigabit transceivers by compensating for operational changes due to cable and circuit characteristics as well as the lengths of connecting cable, by accommodating changes due to manufacturing processes and environmental changes across time and by canceling echoes and correcting for signal offsets, as well as adjusting performance due to direct current and data dependent drifts and off-sets. (Column 3, lines 27-68). It would also have been obvious to a person of ordinary skill in the art that the amplification and equalization performed by the programmable analog front-end are set in accordance with the

programmed deserialization setting so as to be compatible with the deserialization of data.

4. Claims 12, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider in view of Homann and Nagashi et al. (US 2004/0012447 A1, previously cited), hereinafter, Nagashi.

4a. Regarding claim 12, Schneider discloses a programmable logic device (Figs. 4 and 5, transceiver 30. See column 4, lines 54-60 and column 7, lines 27-35. The transceiver is adapted to interface between high-speed serial data having a 1.065GigaHertz data rate and can operate in different modes based on an external MODE signal (hence it is interpreted as being programmable logic device)) comprising:

- clock management module operably coupled to provide a reference clock from clock source (Figs. 4 and 5, TX PLL 40 and RX PLL 48 are interpreted as the clock module. REFCLK is an externally provided signal, generated by a conventional clock circuit. See column 6, line 54- column 7, line 15);
- a transmit module operably coupled to convert transmit parallel data into transmit serial data wherein the transmit PMA module generates the parallel transmit clock, the serial transmit clock, and a transmit programmable logic clock based on the reference clock; (Fig. 5, serializer 52 performs claimed parallel to serial conversion. This conversion is based on the clock provided

by the PLL 40, which in turn is derived from the reference clock (See column 6, line 54- column 7, line 8)) and

- receive module operably coupled to convert receive serial data into receive parallel data, wherein the receive PMA module receives the serial receive data in accordance with a serial receive clock and provides the parallel receive data in accordance with a parallel receive clock, wherein the receive PMA module generates the serial receive clock, the parallel receive clock, and a receive programmable logic clock based on the reference clock ((Fig. 5, deserializer 58 performs claimed parallel to serial conversion (See column 8, lines 1-5)). This conversion is based on the clock provided by the PLL 40, which in turn is derived from the reference clock (See column 7, lines 8-15));
- module operably coupled to convert transmit data words into the transmit parallel data in accordance with parallel receive clock (Column 1, line 65 – column 2, line 15. 8 bit information (claimed transmit data word) is encoded into a 10bit transmission character (claimed transmit parallel data) over the system's parallel architecture in accordance with REFCLK (claimed parallel transmit clock)).
- module to convert the receive parallel data into receive data words in accordance with parallel receive clock (Column 1, line 65 – column 2, line 15. At the receiver, the 10 bit transmission character (obtained after deserialization, interpreted as claimed receive parallel data) is decoded into

an 8-byte recognizable by computer architectures (claimed receive data words) in accordance with REFCLK (claimed parallel receive clock)).

- programmable logic operably produce the transmit data words in accordance with a programmed logic clock and to process receive data words in accordance with parallel receive clock (See column 1, line 25- column 2, line 26. In accordance with the Fibre-Channel physical and signaling interface specification, defined in ANSI X3.230-1994, information to be transmitted over a fibre wire or cable is encoded, 8 bits at a time, into a 10-bit Transmission Character based on REFCLK (claimed logic clock) which is subsequently serially transmitted by bit. Column 1, line 65 – column 2, line 15. At the receiver, the 10 bit transmission character (obtained after deserialization, interpreted as claimed receive parallel data) is decoded into an 8-byte recognizable by computer architectures (claimed receive data words) in accordance with REFCLK (claimed logic clock)).

Scneider further shows an external clock source (Column 6, lines 59-65), recovered clock (Column 7, lines 8-12) and internal clock (Column 1, lines 59-6, wherein self-clocking is interpreted as claimed internal clock). It would have been obvious to a person of ordinary skill in the art to use a low jitter external clock source so that the clock source does add noise to the system.

Thus, Schneider discloses all the limitations of the high-speed transceiver claimed, but fails to explicitly mention the terms programmable physical media attachment (PMA) or programmable physical coding sublayer (PCS), internal

clock. Schneider also fails to explicitly disclose that the reference clock may be chosen from a plurality of clock sources.

In the same field of endeavor, however, Homann discloses a high speed transceiver comprising physical coding sublayer (PCS) device for conversion of data to be transmitted or received to lower layer signals and a physical media attachment device for converting lower layer signals to media signals.(See Paragraphs [0025] and [0026]).

Also in the same field of endeavor, Nagashi discloses a PLL circuit that may be used in a transceiver (paragraph [0006]) a switch (Fig. 1, unit 13) is used in a PLL to choose a reference clock from a plurality of clock sources (Fig. 1, oscillators 12 and 11). (See paragraph [0019]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the terms programmable physical media attachment (PMA) and programmable physical coding sublayer (PCS) (as disclosed by Homann) to describe modules that perform the claimed functions (as shown by Schneider) so as to conform to naming standards.

It would have also been obvious to a person of ordinary skill in the art to use the plurality of clock sources in a clock recovery PLL circuit as shown by Nagashi to improve the performance of the circuit (Paragraph [0022]).

4b. Regarding claim 14, Schneider, Homann and Nagashi disclose all the limitations claimed (See 4a above).

Schneider further discloses programmable logic device wherein the reference clock further comprises:

- a transmit reference clock (Figs. 4 and 5, REFCLK) that is provided to the transmit module, wherein the transmit module generates the serial transmit clock and the parallel transmit clock based on the transmit reference clock (The output of TX PLL is used as clock signal to convert parallel data to serial (claimed serial transmit clock), while the REFCLK itself is used to encode parallel data (claimed parallel transmit clock)); and
- a receive reference clock (Figs. 4 and 5, REFCLK) that is provided to the receive PMA module, wherein the receive PMA module generates the serial receive clock and the parallel receive clock based on the receive reference clock (The output of RX PLL is used as clock signal to convert serial data to parallel (claimed serial receive clock), while the REFCLK itself is used to decode parallel data (claimed parallel receive clock)).

4c. Regarding claim 16, Schneider, Homann and Nagashi show all the limitations claimed (See 4a above).

Schneider further shows the programmable gigabit transceiver wherein the programmable PMA transmitter module further comprises:

- phase locked loop operably coupled to produce serial transmit clock, parallel transmit clock and transmit programmable logic clock based on the reference clock in accordance with a programmed serialized setting (See Fig. 4 and

column 6, line 46 – column 7, line 8. Transmitter phase locked loop 40 produces the required 1.0625 GHz serial signal clock (claimed serial transmit clock) defining the data rate of the high speed output, i.e. in accordance with the programmed serialization setting, as claimed. REFCLK itself is used as claimed transmit parallel clock and logic clock);

- parallel-to-serial module operably coupled to convert the transmit parallel data into the transmit serial data based on the timing signals, wherein data width of the transmit parallel data and rate of the transmit serial data are set in accordance with the programmed serialization setting; (See Fig. 4 and column 7, lines 48-58. Once a 10-bit transmission character is latched into the transmitter section 38 through input latch 50, the transmission character is serialized in serializer 52, operating in accordance with a 1.0625 GHz signal provided by the transmitter PLL 40. Thus, parallel data and rate of the transmit serial data are set in accordance with the 1.0625 GHz timing signal. Since the 1.0625 GHz timing signal is set in accordance with the programmed serialized setting, data width of the transmit parallel data and rate of the transmit serial data are also set in accordance with the programmed serialization setting, as claimed); and
- driver operably coupled to drive the transmit serial data on to a transmission line, wherein drive level of the driver and pre-emphasis settings of the driver is set in accordance with the programmed serialization setting (See Fig. 4 and column 7, lines 48-58. Once serialized, a 1.0625 GHz serial datastream is

directed out of the transmitter section 38 through an output buffer 54 (interpreted as claimed driver) which matches the serial data signal characteristics to the requirements of the Fibre Channel transmission bus (claimed transmission line), i.e. Output buffer 54 performs the function of claimed driver by outputting data onto the Fibre Channel transmission bus (claimed transmission line) in accordance with the serial data signal characteristics (claimed serialized setting)).

5. Claims 15, rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider, Homann and Nagashi as applied to claim 12 above, and further in view of Phanse.

5a. Regarding claim 15, Schneider, Homann and Nagashi disclose all the limitations claimed (See 4a above).

Schneider further discloses the programmable logic device wherein the programmable receiver module further comprises:

data and clock recovery module operably coupled to recover data and a clock receive serial data to produce recovered data and a recovered clock, respectively, wherein the data and clock recovery module includes a programmable phase locked loop that is programmed in accordance with the programmed deserialization setting; and serial-to-parallel module operably coupled to convert the recovered data into the receive parallel data, wherein rate

of the receive parallel data and width of the receive parallel data are set in accordance with the programmed deserialization setting. (A receiver section 44 is coupled to a high speed serial data input 46 and further comprises a receiver phase lock loop 48 (claimed data and clock recover module) which locks on to a 1.0625 GHz incoming serial signal and recovers a high speed serial clock and data. Serial data is converted into 10-bit parallel data (interpreted as claimed serial-to-parallel module) and the recovered parallel data is provided to the protocol device 32 over the 10-bit wide parallel TTL data receiver bus 36. See Fig 5 and column 7, lines 8-15).

Thus, Schneider and Homann disclose all the limitations claimed, but fail to explicitly disclose the claimed analog from end.

However, in the same field of endeavor, Phanse shows a gigabit rate transceiver with an analog front end operably coupled to:

- amplify and equalize the receive serial data to produce amplified and equalized receive serial data(Phanse's analog front end comprises an automatic gain control (AGC) circuit capable of receiving the reduced-echo incoming analog signal and amplifying the reduced-echo incoming analog signal by an adjustable gain factor (thus interpreted as programmable amplification, as claimed) to thereby produce an amplified incoming analog signal and an adaptive analog equalization filter capable of receiving the incoming amplified analog signal and amplifying a first high frequency

component of the amplified incoming analog signal to thereby produce an analog filtered incoming signal Column 3, lines 45-68).

Thus, it would have been obvious to a person of ordinary skill in the art to use the analog front-end disclosed by Phanse because it improves performance of gigabit transceivers by compensating for operational changes due to cable and circuit characteristics as well as the lengths of connecting cable, by accommodating changes due to manufacturing processes and environmental changes across time and by canceling echoes and correcting for signal offsets, as well as adjusting performance due to direct current and data dependent drifts and off-sets. (Column 3, lines 27-68). It would also have been obvious to a person of ordinary skill in the art that the amplification and equalization performed by the programmable analog front-end are set in accordance with the programmed deserialization setting so as to be compatible with the deserialization of data.

6. Claims 28, 40 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider in view of Agazzi et al. (US 2001/0055331 A1, previously cited), hereinafter, Agazzi.

6a. Regarding claim 28, Schneider discloses a programmable logic device (Figs. 4 and 5, transceiver 30. See column 4, lines 54-60 and column 7, lines 27-35. The transceiver is adapted to interface between high-speed serial data having a

1.065GigaHertz data rate (hence interpreted as claimed gigabit transceiver) and can operate in different modes based on an external MODE signal (hence it is interpreted as being programmable)) comprising:

- programmable gigabit transceivers is individually programmed to a desired transceiving mode of operation in accordance with a plurality of transceiver settings to transceive data; programmable logic fabric operably coupled to the programmable gigabit transceiver, wherein the programmable logic fabric is configured to process at least a portion of the data; and control module operably coupled to produce transceiver settings based on a desired mode of operation of the programmable logic device (See Figs. 4 and 5; column 7, lines 27-35. MODE is an external signal, typically asserted via controller circuitry (claimed control module) operating under software or firmware program control, in response to certain predetermined conditions. Thus, MODE controls the operation of the transceiver and so the transceiver is interpreted as being programmed to a desired mode of operation, as claimed. The data is processed by the Fibre Channel protocol device 32 (Fig. 4) See column 6, lines 40-65 and the transmitter 38 and receiver 44);

Thus, Schneider discloses all the limitations of the high-speed transceiver claimed, but fails to explicitly mention whether the transceivers may be multi-gigabit transceivers and whether there may be a plurality of such transceivers.

In the same field of endeavor, however, Agazzi discloses a multi-gigabit transceiver system having a plurality of multi-gigabit transceivers (Fig. 1, paragraph [0096]).

Thus, it would have been obvious to a person of ordinary skill in the art that Schneider's transceiver may be a multi-gigabit transceiver so as to increase system capacity and that the transceiver may be on a device comprising a plurality of such transceivers as shown by Agazzi so to ensure fast and effective communication between the plurality of transceivers.

6b. Regarding claim 40, Schneider and Agazzi disclose all the limitations claimed (see 6a above). Schneider further discloses gigabit transceiver comprising:

- transmit section operably coupled to convert transmit data words into transmit serial data in accordance with a transmit setting (Fig. 5, transmitter 38 comprises serializer 52 performs claimed parallel to serial conversion (See column 7, lines 49-52). Also see column 1, line 65 – column 2, line 15. 8bit information (claimed transmit data word) is encoded into a 10bit transmission character (claimed transmit parallel data))
- a receive section operably coupled to convert receive serial data stream into receive data words in accordance with a receive setting ((Fig. 5, Receiver 44 comprises deserializer 58 performs claimed parallel to serial conversion (See column 8, lines 1-5). Also see column 1, line 65 – column 2, line 15. The 10 bit transmission character (obtained after deserialization, interpreted as

claimed receive parallel data) is decoded into an 8-byte recognizable by computer architectures (claimed receive data words));

- module operably coupled to convert transmit data words into the transmit parallel data in accordance with a transmit interface setting and to convert the receive parallel data into receive data words in accordance with a receive interface setting (Column 1, line 65 – column 2, line 15. 8bit information (claimed transmit data word) is encoded into a 10bit transmission character (claimed transmit parallel data) over the system's parallel architecture. Similarly, at the receiver, the 10 bit transmission character (obtained after deserialization, interpreted as claimed receive parallel data) is decoded into an 8-byte recognizable by computer architectures (claimed receive data words). Fig. 4. The Fibre Channel protocol device 32 performs the encoding and is interpreted as claimed module. See column 6, lines 40-65);
- an interface to programmable logic section operably coupled to provide the transmit data words from the programmable logic section to the transmit section in accordance with the transmit setting and to receive the receive data words from the receive section in accordance with the receive setting (See column 1, line 25- column 2, line 26. In accordance with the Fibre-Channel physical and signaling interface specification, defined in ANSI X3.230-1994, information to be transmitted over a fibre wire or cable is encoded, 8 bits at a time, into a 10-bit Transmission Character which is subsequently serially transmitted by bit. Data provided over a typical computer system's parallel

architecture is encoded and framed such that each data byte (8-bits from the point of view of the computer system) is formed into a Transmission Character in accordance with the Fibre-Channel 8B/10B transmission code. See Fig. 4. Since the Fibre Channel protocol device 32 performs the encoding, it inherently interfaces the data to be transmitted (claimed transmit data words) to the transceiver by performing the 8B/10B encoding on the data to be transmitted (to form claimed transmit parallel data). Similarly, the encoded received data (claimed received parallel words) is decoded by the Fibre Channel protocol device 32 and delivered in decoded form (claimed received data words). Thus, the Fibre-Channel protocol device is interpreted as claimed programmable interface. See column 6, lines 40-65); and

- control module operably coupled to produce the transmit setting and the receive setting based on transceiver operational requirements (See Figs. 4 and 5; column 7, lines 27-35. MODE is an external signal, typically asserted via controller circuitry (claimed control module) operating under software or firmware program control, in response to certain predetermined conditions).

6c. Regarding claim 47, Schneider and Agazzi show all the limitations claimed (See 2e above).

Schneider further shows the control module further functions to:

- receive a programming setting that indicates the desired mode of operation for the programmable gigabit transceiver (See Figs. 4 and 5; column 7, lines 27-35.

MODE is an external signal, typically asserted via controller circuitry (claimed control module) operating under software or firmware program control, in response to certain predetermined conditions. Thus, MODE indicates the desired mode of operation of the programmable gigabit transceiver).

- convert the programming setting into the programmed receive setting, and transmit setting, (Since the gigabit transceiver operates based on the received MODE signal, the MODE signal inherently gets converted into claimed transmit and receive settings);

7. Claims 29-33, 36, 37, 41, 42 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider and Agazzi as applied to claims 28 and 40 above, and further in view of Homann.

7a. Regarding claim 29, Schneider and Agazzi disclose all the limitations claimed (See 6 a above). Schneider further shows individual transceiver comprising:

- a module operably coupled to convert transmit parallel data into transmit serial data in accordance with a programmed serialization setting (Fig. 5, serializer 52 performs claimed parallel to serial conversion (See column 7, lines 49-52)) and to convert receive serial data into receive parallel data in accordance with a programmed deserialization setting ((Fig. 5, deserializer 58 performs claimed parallel to serial conversion (See column 8, lines 1-5)));

- module operably coupled to convert transmit data words into the transmit parallel data in accordance with a transmit interface setting and to convert the receive parallel data into receive data words in accordance with a receive interface setting (Column 1, line 65 – column 2, line 15. 8bit information (claimed transmit data word) is encoded into a 10bit transmission character (claimed transmit parallel data) over the system's parallel architecture. Similarly, at the receiver, the 10 bit transmission character (obtained after deserialization, interpreted as claimed receive parallel data) is decoded into an 8-byte recognizable by computer architectures (claimed receive data words). Fig. 4. The Fibre Channel protocol device 32 performs the encoding and is interpreted as claimed module. See column 6, lines 40-65);
- programmable interface operably to convey the receive data words and to convey the transmit data words in accordance with a programmed logic interface setting (See column 1, line 25- column 2, line 26. In accordance with the Fibre-Channel physical and signaling interface specification, defined in ANSI X3.230-1994, information to be transmitted over a fibre wire or cable is encoded, 8 bits at a time, into a 10-bit Transmission Character which is subsequently serially transmitted by bit. Data provided over a typical computer system's parallel architecture is encoded and framed such that each data byte (8-bits from the point of view of the computer system) is formed into a Transmission Character in accordance with the Fibre-Channel 8B/10B transmission code. See Fig. 4. Since the Fibre Channel protocol

device 32 performs the encoding, it inherently interfaces the data to be transmitted (claimed transmit data words) to the transceiver by performing the 8B/10B encoding on the data to be transmitted (to form claimed transmit parallel data). Similarly, the encoded received data (claimed received parallel words) is decoded by the Fibre Channel protocol device 32 and delivered in decoded form (claimed received data words). Thus, the Fibre-Channel protocol device is interpreted as claimed programmable interface. See column 6, lines 40-65); and

Thus, Schneider discloses all the limitations of the high-speed transceiver claimed, but neither Schneider nor Agazzi explicitly mention the terms programmable physical media attachment (PMA) or programmable physical coding sublayer (PCS).

In the same field of endeavor, however, Homann discloses a high speed transceiver comprising physical coding sublayer (PCS) device for conversion of data to be transmitted or received to lower layer signals and a physical media attachment device for converting lower layer signals to media signals.(See Paragraphs [0025] and [0026]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the terms programmable physical media attachment (PMA) and programmable physical coding sublayer (PCS) (as disclosed by Homann) to describe modules that perform the claimed functions (as shown by Schneider) so as to conform to naming standards.

7b. Regarding claim 30, Schneider, Agazzi and Homann show all the limitations claimed (See 7a above).

Schneider further shows the programmable gigabit transceiver wherein the programmable module comprises:

- a programmable receiver module operably coupled to convert the serial data in accordance with the programmed deserialization setting to produce the receive parallel data; and (Fig. 5, deserializer 58 performs claimed deserialization in the receiver section 44 (claimed receiver module) of transceiver. See column 8, lines 1-5);
- a programmable transmitter module operably coupled to convert the transmit parallel data in accordance with a programmed serialization setting to produce the transmit serial data. (Fig. 5, serializer 52 performs claimed serialization in the transmitter section 38 (claimed transmitter module) of transceiver. See column 7, lines 49-52).

7c. Regarding claim 31, Schneider, Agazzi and Homann disclose all the limitations claimed (See 7b above).

Schneider further discloses the programmable gigabit transceiver wherein the programmable receiver module further comprises:

data and clock recovery module operably coupled to recover data and a clock receive serial data to produce recovered data and a recovered clock,

respectively, wherein the data and clock recovery module includes a programmable phase locked loop that is programmed in accordance with the programmed deserialization setting; and serial-to-parallel module operably coupled to convert the recovered data into the receive parallel data, wherein rate of the receive parallel data and width of the receive parallel data are set in accordance with the programmed deserialization setting. (A receiver section 44 is coupled to a high speed serial data input 46 and further comprises a receiver phase lock loop 48 (claimed data and clock recover module) which locks on to a 1.0625 GHz incoming serial signal and recovers a high speed serial clock and data. Serial data is converted into 10-bit parallel data (interpreted as claimed serial-to-parallel module) and the recovered parallel data is provided to the protocol device 32 over the 10-bit wide parallel TTL data receiver bus 36. See Fig 5 and column 7, lines 8-15).

Thus, Schneider and Homann disclose all the limitations claimed, but fail to explicitly disclose the claimed analog from end.

However, in the same field of endeavor, Phanse shows a gigabit rate transceiver with an analog front end operably coupled to:

- amplify and equalize the receive serial data to produce amplified and equalized receive serial data(Phanse's analog front end comprises an automatic gain control (AGC) circuit capable of receiving the reduced-echo incoming analog signal and amplifying the reduced-echo incoming analog signal by an adjustable gain factor (thus interpreted as programmable

amplification, as claimed) to thereby produce an amplified incoming analog signal and an adaptive analog equalization filter capable of receiving the incoming amplified analog signal and amplifying a first high frequency component of the amplified incoming analog signal to thereby produce an analog filtered incoming signal Column 3, lines 45-68).

Thus, it would have been obvious to a person of ordinary skill in the art to use the analog front-end disclosed by Phanse because it improves performance of gigabit transceivers by compensating for operational changes due to cable and circuit characteristics as well as the lengths of connecting cable, by accommodating changes due to manufacturing processes and environmental changes across time and by canceling echoes and correcting for signal offsets, as well as adjusting performance due to direct current and data dependent drifts and off-sets. (Column 3, lines 27-68). It would also have been obvious to a person of ordinary skill in the art that the amplification and equalization performed by the programmable analog front-end are set in accordance with the programmed deserialization setting so as to be compatible with the deserialization of data.

7d. Regarding claim 32, Schneider, Agazzi and Homann show all the limitations claimed (See 7b above).

Schneider further shows the programmable gigabit transceiver wherein the programmable PMA transmitter module further comprises:

- phase locked loop operably coupled to produce timing signals in accordance with the programmed serialization setting (See Fig. 4 and column 6, line 46 – column 7, line 8. Transmitter phase locked loop 40 produces the required 1.0625 GHz serial signal clock (claimed timing signal) defining the data rate of the high speed output, i.e. in accordance with the programmed serialization setting, as claimed);
- parallel-to-serial module operably coupled to convert the transmit parallel data into the transmit serial data based on the timing signals, wherein data width of the transmit parallel data and rate of the transmit serial data are set in accordance with the programmed serialization setting; (See Fig. 4 and column 7, lines 48-58. Once a 10-bit transmission character is latched into the transmitter section 38 through input latch 50, the transmission character is serialized in serializer 52, operating in accordance with a 1.0625 GHz signal provided by the transmitter PLL 40. Thus, parallel data and rate of the transmit serial data are set in accordance with the 1.0625 GHz timing signal. Since the 1.0625 GHz timing signal is set in accordance with the programmed serialized setting, data width of the transmit parallel data and rate of the transmit serial data are also set in accordance with the programmed serialization setting, as claimed); and
- driver operably coupled to drive the transmit serial data on to a transmission line, wherein drive level of the driver and pre-emphasis settings of the driver is set in accordance with the programmed serialization setting (See Fig. 4 and

column 7, lines 48-58. Once serialized, a 1.0625 GHz serial datastream is directed out of the transmitter section 38 through an output buffer 54 (interpreted as claimed driver) which matches the serial data signal characteristics to the requirements of the Fibre Channel transmission bus (claimed transmission line), i.e. Output buffer 54 performs the function of claimed driver by outputting data onto the Fibre Channel transmission bus (claimed transmission line) in accordance with the serial data signal characteristics (claimed serialized setting)).

7e. Regarding claim 33, Schneider and Homann show all the limitations claimed (See 7a above).

Schneider further shows the programmable gigabit transceiver wherein the programmable module comprises:

- a programmable receive module operably coupled to convert the receive parallel data into receive data words in accordance with the receive interface setting; and a programmable PCS transmit module operably coupled to convert the transmit data words into the transmit parallel data in accordance with the transmit interface setting. (Column 1, line 65 – column 2, line 15. At the transmitter (claimed transmit module), 8bit information (claimed transmit data word) is encoded into a 10bit transmission character (claimed transmit parallel data) over the system's parallel architecture. Similarly, at the receiver (claimed receive module), the 10 bit transmission character (obtained after

deserialization, interpreted as claimed receive parallel data) is decoded into an 8-byte recognizable by computer architectures (claimed receive data words). Fig. 4. The Fibre Channel protocol device 32 performs the encoding. See column 6, lines 40-65).

7f. Regarding claim 36, Schneider, Agazzi and Homann show all the limitations claimed (See 7a above).

Since Schneider discloses a programmable gigabit transceiver (See 2a above), memory to store the programmed settings is inherent.

Thus, Schneider discloses all the limitations of the high-speed transceiver claimed, but fails to explicitly mention the terms programmable physical media attachment (PMA) or programmable physical coding sublayer (PCS).

In the same field of endeavor, however, Homann discloses a high speed transceiver comprising physical coding sublayer (PCS) device for conversion of data to be transmitted or received to lower layer signals and a physical media attachment device for converting lower layer signals to media signals.(See Paragraphs [0025] and [0026]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the terms programmable physical media attachment (PMA) and programmable physical coding sublayer (PCS) (as disclosed by Homann) to describe modules that perform the claimed functions (as shown by Schneider) so as to conform to naming standards. It would have also been obvious to a person of ordinary skill

in the art to use separate memory registers for the PMA and PCS settings, because this would ensure dedicated registers for each module, resulting in faster and easier memory access.

7g. Regarding claim 37, Schneider, Agazzi and Homann show all the limitations claimed (See 7a above).

Schneider further shows the control module further functions to:

- receive a programming setting that indicates the desired mode of operation for the programmable gigabit transceiver (See Figs. 4 and 5; column 7, lines 27-35. MODE is an external signal, typically asserted via controller circuitry (claimed control module) operating under software or firmware program control, in response to certain predetermined conditions. Thus, MODE indicates the desired mode of operation of the programmable gigabit transceiver).
  - convert the programming setting into the programmed serialization setting, the programmed deserialization setting, the receive interface setting, the transmit interface setting, and the logic interface setting (Since the gigabit transceiver operates based on the received MODE signal, the MODE signal inherently gets converted into serialization setting, deserialization setting and the interface setting, so as to control the serializer , deserializer and interface);

Since Schneider discloses a programmable gigabit transceiver (See 2a above), memory to store the programmed settings is inherent.

Thus, Schneider discloses all the limitations of the high-speed transceiver claimed, but fails to explicitly mention the terms programmable physical media attachment (PMA) register or programmable physical coding sublayer (PCS) register.

In the same field of endeavor, however, Homann discloses a high speed transceiver comprising physical coding sublayer (PCS) device for conversion of data to be transmitted or received to lower layer signals and a physical media attachment device for converting lower layer signals to media signals.(See Paragraphs [0025] and [0026]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the terms programmable physical media attachment (PMA) and programmable physical coding sublayer (PCS) (as disclosed by Homann) to describe modules that perform the claimed functions (as shown by Schneider) so as to conform to naming standards. It would have also been obvious to a person of ordinary skill in the art to use separate memory registers for the PMA and PCS settings, because this would ensure dedicated registers for each module, resulting in faster and easier memory access.

7h. Regarding claim 41, Schneider and Agazzi disclose all the limitations claimed, including the conversion of transmit data words into transmit parallel data and

serializing of the parallel data in accordance with a transmit setting (See 6a above).

However, both Schneider and Agazzi fail to explicitly mention the terms programmable physical media attachment (PMA) or programmable physical coding sublayer (PCS).

In the same field of endeavor, however, Homann discloses a high speed transceiver comprising physical coding sublayer (PCS) device for conversion of data to be transmitted or received to lower layer signals and a physical media attachment device for converting lower layer signals to media signals.(See Paragraphs [0025] and [0026]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the terms programmable physical media attachment (PMA) and programmable physical coding sublayer (PCS) (as disclosed by Homann) to describe modules that perform the claimed functions (as shown by Schneider) so as to conform to naming standards.

7i. Regarding claim 42, Schneider, Agazzi and Homann show all the limitations claimed (See 7h above).

Schneider further shows the programmable gigabit transceiver wherein the programmable PMA transmitter module further comprises:

- phase locked loop operably coupled to produce timing signals in accordance with the transmit setting (See Fig. 4 and column 6, line 46 – column 7, line 8.

Transmitter phase locked loop 40 produces the required 1.0625 GHz serial signal clock (claimed timing signal) defining the data rate of the high speed output, i.e. in accordance with the programmed serialization setting, as claimed);

- parallel-to-serial module operably coupled to convert the transmit parallel data into the transmit serial data based on the transmit setting, wherein data width of the transmit parallel data and rate of the transmit serial data are set in accordance with the transmit setting; (See Fig. 4 and column 7, lines 48-58. Once a 10-bit transmission character is latched into the transmitter section 38 through input latch 50, the transmission character is serialized in serializer 52, operating in accordance with a 1.0625 GHz signal provided by the transmitter PLL 40. Thus, parallel data and rate of the transmit serial data are set in accordance with the 1.0625 GHz timing signal. Since the 1.0625 GHz timing signal is set in accordance with the programmed serialized setting, data width of the transmit parallel data and rate of the transmit serial data are also set in accordance with the transmit setting, as claimed); and
- driver operably coupled to drive the transmit serial data on to a transmission line, wherein drive level of the driver and pre-emphasis settings of the driver is set in accordance with the transmit setting (See Fig. 4 and column 7, lines 48-58. Once serialized, a 1.0625 GHz serial datastream is directed out of the transmitter section 38 through an output buffer 54 (interpreted as claimed driver) which matches the serial data signal characteristics to the

requirements of the Fibre Channel transmission bus (claimed transmission line), i.e. Output buffer 54 performs the function of claimed driver by outputting data onto the Fibre Channel transmission bus (claimed transmission line) in accordance with the serial data signal characteristics (claimed serialized setting) at the transmitter, i.e. in accordance with the transmit setting).

7j. Regarding claim 44, Schneider and Agazzi disclose all the limitations claimed, including the conversion of receive serial data into receive parallel data and subsequently to receive data word in accordance with a receive setting (See 6b above).

However, Schneider and Agazzi fail to explicitly mention the terms programmable physical media attachment (PMA) or programmable physical coding sublayer (PCS).

In the same field of endeavor, however, Homann discloses a high speed transceiver comprising physical coding sublayer (PCS) device for conversion of data to be transmitted or received to lower layer signals and a physical media attachment device for converting lower layer signals to media signals.(See Paragraphs [0025] and [0026]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the terms programmable physical media attachment (PMA) and programmable physical coding sublayer (PCS) (as disclosed by Homann) to describe modules

that perform the claimed functions (as shown by Schneider) so as to conform to naming standards.

8. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider, Agazzi and Homann as applied to claim 44 above, and further in view of Phanse.

8a Regarding claim 45, Schneider, Agazzi and Homann disclose all the limitations claimed (See 7j above).

Schneider further discloses the programmable gigabit transceiver wherein the programmable receiver module further comprises:

data and clock recovery module operably coupled to recover data and a clock receive serial data to produce recovered data and a recovered clock, respectively, wherein the data and clock recovery module includes a programmable phase locked loop that is programmed in accordance with the receiver setting; and serial-to-parallel module operably coupled to convert the recovered data into the receive parallel data, wherein rate of the receive parallel data and width of the receive parallel data are set in accordance with the programmed receive setting. (A receiver section 44 is coupled to a high speed serial data input 46 and further comprises a receiver phase lock loop 48 (claimed data and clock recover module) which locks on to a 1.0625 GHz incoming serial signal and recovers a high speed serial clock and data. Serial data is converted

into 10-bit parallel data (interpreted as claimed serial-to-parallel module) and the recovered parallel data is provided to the protocol device 32 over the 10-bit wide parallel TTL data receiver bus 36. See Fig 5 and column 7, lines 8-15).

Thus, Schneider, Agazzi and Homann disclose all the limitations claimed, but fail to explicitly disclose the claimed analog from end.

However, in the same field of endeavor, Phanse shows a gigabit rate transceiver with an analog front end operably coupled to:

- amplify and equalize the receive serial data to produce amplified and equalized receive serial data(Phanse's analog front end comprises an automatic gain control (AGC) circuit capable of receiving the reduced-echo incoming analog signal and amplifying the reduced-echo incoming analog signal by an adjustable gain factor (thus interpreted as programmable amplification, as claimed) to thereby produce an amplified incoming analog signal and an adaptive analog equalization filter capable of receiving the incoming amplified analog signal and amplifying a first high frequency component of the amplified incoming analog signal to thereby produce an analog filtered incoming signal Column 3, lines 45-68).

Thus, it would have been obvious to a person of ordinary skill in the art to use the analog front-end disclosed by Phanse because it improves performance of gigabit transceivers by compensating for operational changes due to cable and circuit characteristics as well as the lengths of connecting cable, by accommodating changes due to manufacturing processes and environmental

changes across time and by canceling echoes and correcting for signal offsets, as well as adjusting performance due to direct current and data dependent drifts and off-sets. (Column 3, lines 27-68). It would also have been obvious to a person of ordinary skill in the art that the amplification and equalization performed by the programmable analog front-end are set in accordance with the programmed deserialization setting so as to be compatible with the deserialization of data.

Allowable Subject Matter

9. Claims 19-26 are allowed.

The following is an examiner's statement of reasons for allowance:

9a. Regarding claim 19, prior art of record fails to show the programmable multi-gigabit transceiver, wherein the control module further functions to: generate the receive setting to enable, logically disable, or physically disable at least one element of a programmable PMA receiver module of the receiver section; generate the transmit setting to enable, logically disable, or physically disable at least one element of a programmable PMA transmit module of the transmit section; generate the transmit setting to enable, logically disable, or physically disable at least one element of a programmable PCS transmit module of the transmit section; and generate the receive setting to enable, logically disable, or physically disable at least one element of a programmable PCS receive module

of the receive section, in combination with each and every other limitation of the claim.

9b. Claims 20-26 are allowed as being dependent on claim 19.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

10. Claims 6, 7, 10, 11,17, 18, 34, 35, 38, 39, 43, 46 and 48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10a. Regarding claims 6, prior art of record fails to show the programmable multi-gigabit transceiver, wherein the programmable PCS receive module further comprises: programmable descramble and decode module operably coupled to descramble, decode, or pass the aligned data words in accordance with the receive interface setting to produce processed aligned data words, wherein the receive interface setting indicates descrambling, decoding, or passing of the aligned data words, wherein the receive interface setting further indicates a type of descrambling when the programmable descramble and decode module is descrambling the aligned data words and further indicates a type of decoding

when the programmable descramble and decode module is decoding the aligned data words, in combination with each and every other limitation of the claim and it's base claim.

10b. Regarding claim 6, prior art of record fails to show the programmable multi-gigabit transceiver, wherein programmable scrambling module operably coupled to scramble or pass the stored encoded data words in accordance with the transmit interface setting to produce the transmit parallel data, wherein the transmit interface setting indicates a type of scrambling when the programmable scrambling module is scrambling the stored encoded data words, in combination with each and every other limitation of the claim and it's base claim.

10c. Regarding claim 10, prior art of record fails to show the programmable multi-gigabit transceiver, wherein the control module further functions to: determine a programming setting that indicates the desired mode of operation for the programmable multi-gigabit transceiver based on auto-configuration information; convert the programming setting into the programmed serialization setting, the programmed deserialization setting, the receive interface setting, the transmit interface setting, and the logic interface setting; provide the programmed serialization setting and the programmed deserialization setting to the PMA memory mapped register; and provide the transmit and receive interface settings

and the programmed logic interface setting to the PCS register, <u>in combination with each and every other limitation of the claim and it's base claim</u>.

10d. Regarding claim 11, prior art of record fails to show the programmable multi-gigabit transceiver, wherein the control module further functions to: generate the receive setting to enable, logically disable, or physically disable at least one element of a programmable PMA receiver module of the receiver section; generate the transmit setting to enable, logically disable, or physically disable at least one element of a programmable PMA transmit module of the transmit section; generate the transmit setting to enable, logically disable, or physically disable at least one element of a programmable PCS transmit module of the transmit section; and generate the receive setting to enable, logically disable, or physically disable at least one element of a programmable PCS receive module of the receive section, <u>in combination with each and every other limitation of the base claim</u>.

10e. Regarding claims 17, prior art of record fails to show the programmable multi-gigabit transceiver, wherein programmable descramble and decode module operably coupled to descramble, decode, or pass the aligned data words in accordance with the receive interface setting to produce processed aligned data words, wherein the receive interface setting indicates descrambling, decoding, or

passing of the aligned data words, wherein the receive interface setting further indicates a type of descrambling when the programmable descramble and decode module is descrambling the aligned data words and further indicates a type of decoding when the programmable descramble and decode module is decoding the aligned data words in combination with each and every other limitation of the claim and it's base claim.

10f. Regarding claims 17, prior art of record fails to show the programmable multi-gigabit transceiver, wherein programmable scrambling module operably coupled to scramble or pass the stored encoded data words in accordance with the transmit interface setting to produce the parallel transmit data, wherein the transmit interface setting indicates a type of scrambling when the programmable scrambling module is scrambling the stored encoded data words, in combination with each and every other limitation of the claim and it's base claim.

10g. Regarding claim 34, prior art of record fails to show the programmable device comprises programmable descramble and decode module operably coupled to descramble, decode, or pass the aligned data words in accordance with the receive PMA_PCS interface setting to produce processed aligned data words, wherein the receive PMA_PCS interface setting indicates descrambling, decoding, or passing of the aligned data words, wherein the receive PMA_PCS interface setting further indicates a type of descrambling when the programmable

descramble and decode module is descrambling the aligned data words and further indicates a type of decoding when the programmable descramble and decode module is decoding the aligned data words, in combination with each and every other limitation of the claim and it's base claims.

10h. Regarding claim 34, prior art of record fails to show the programmable device comprises programmable scrambling module operably coupled to scramble or pass the stored encoded data words in accordance with the transmit PMA_PCS interface setting to produce the transmit parallel data, wherein the transmit PMA_PCS interface setting indicates a type of scrambling when the programmable scrambling module is scrambling the stored encoded data words, in combination with each and every other limitation of the claim and it's base claims.

10i. Regarding claim 38, prior art of record fails to show the programmable device wherein control module is configured to determine a programming setting that indicates the desired mode of operation for the programmable multi-gigabit transceiver based on auto-configuration information; convert the programming setting into the programmed serialization setting, the programmed deserialization setting, the receive PMA_PCS interface setting, the transmit PMA_PCS interface setting, and the logic interface setting; provide the programmed serialization setting and the programmed deserialization setting to the PMA memory mapped

register; and provide the transmit and receive PMA_PCS interface settings and the programmed logic interface setting to the PCS register, <u>in combination with each and every other limitation of the claim and it's base claims</u>.

10j. Regarding claim 39, prior art of record fails to show the programmable logic device, wherein the control module further functions to: generate the programmed serialization setting to enable, logically disable, or physically disable at least one element of a programmable PMA receiver module of the programmable PMA module; generate the programmed deserialization setting to enable, logically disable, or physically disable at least one element of a programmable PMA transceiver module of the programmable PMA module; generate the transmit PMA_PCS interface setting to enable, logically disable, or physically disable at least one element of a programmable PCS transmit module of the programmable PCS module; and generate the receive PMA_PCS interface setting to enable, logically disable, or physically disable at least one element of a programmable PCS receive module of the programmable PCS module, <u>in combination with each and every other limitation of the claim and it's base claims</u>.

10k. Regarding claim 43, prior art of record fails to show the programmable logic device, comprising programmable scrambling module operably coupled to scramble or pass the stored encoded data words in accordance with the transmit setting to produce the transmit parallel data, wherein the transmit setting indicates a type of scrambling when the programmable scrambling module is scrambling the stored encoded data words, in combination with each and every other limitation of the claim and it's base claims.

10l. Regarding claim 46, prior art of record fails to show the programmable logic device, comprising programmable descramble and decode module operably coupled to descramble, decode, or pass the aligned data words in accordance with the receive setting to produce processed aligned data words, wherein the receive setting indicates descrambling, decoding, or passing of the aligned data words, wherein the receive setting further indicates a type of descrambling when the programmable descramble and decode module is descrambling the aligned data words and further indicates a type of decoding when the programmable descramble and decode module is decoding the aligned data words; programmable storage module operably coupled to elastic store or pass the processed data words in accordance with the receive setting to produce stored data words, in combination with each and every other limitation of the claim and it's base claims.

10m. Regarding claim 48, prior art of record fails to show the programmable logic device, wherein the control module further functions to: generate the receive setting to enable, logically disable, or physically disable at least one element of a programmable PMA receiver module of the receiver section; generate the transmit setting to enable, logically disable, or physically disable at least one element of a programmable PMA transceiver module of the transmit section; generate the transmit setting to enable, logically disable, or physically disable at least one element of a programmable PCS transmit module of the transmit section; and generate the receive setting to enable, logically disable, or physically disable at least one element of a programmable PCS receive module of the receive section, in combination with each and every other limitation of the claim and it's base claims.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vineeta S. Panwalkar whose telephone number is 571-272-8561. The examiner can normally be reached on M-F 8:30-5:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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